

General Description

The GreenMOS[®] MOSFET utilizes charge balance technology to achieve outstanding low on-resistance and lower gate charge. It is engineered to minimize conduction loss, provide superior switching performance and robust avalanche capability.

The GreenMOS[®] Generic series is optimized for extreme switching performance to minimize switching loss. It is tailored for high power density applications to meet the highest efficiency standards.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity

GreenMOS[®]



Applications

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- PFC Circuits

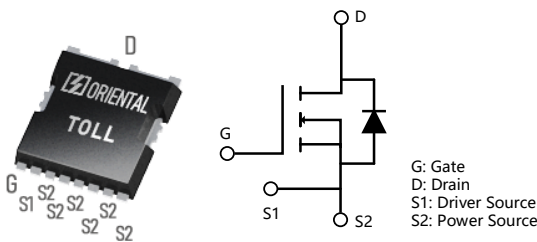
Key Performance Parameters

Parameter	Value	Unit
V_{DS}	300	V
I_D, pulse	156	A
$R_{DS(ON), \text{max}} @ V_{GS}=10V$	25	m Ω
Q_g	54	nC

Marking Information

Product Name	Package	Marking
OSG30R025TF	TOLL	OSG30R025T

Package & Pin Information



Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	300	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	78	A
Continuous drain current ¹⁾ , $T_C=100^\circ\text{C}$		49	
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D, pulse}$	156	A
Continuous diode forward current ¹⁾ , $T_C=25^\circ\text{C}$	I_S	78	A
Diode pulsed current ²⁾ , $T_C=25^\circ\text{C}$	$I_{S, pulse}$	156	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	357	W
Single pulsed avalanche energy ⁴⁾	E_{AS}	800	mJ
Reverse diode dv/dt	dv/dt	50	V/ns
Operation and storage temperature	T_{stg}, T_j	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.35	$^\circ\text{C/W}$
Thermal resistance, junction-ambient	$R_{\theta JA}$	62	$^\circ\text{C/W}$

Electrical Characteristics at $T_j=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	300			V	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3		5	V	$V_{DS}=V_{GS}, I_D=1\text{ mA}$
Drain-source on-state resistance	$R_{DS(ON)}$		18.6	25	m Ω	$V_{GS}=10\text{ V}, I_D=39\text{ A}$
			43.3			$V_{GS}=10\text{ V}, I_D=39\text{ A}, T_j=150^\circ\text{C}$
Transconductance	g_{fs}	28	47		S	$V_{DS} = 10\text{ V}, I_D = 39\text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			10	μA	$V_{DS}=300\text{ V}, V_{GS}=0\text{ V}$
Gate resistance	R_G		4.8		Ω	$f=1\text{ MHz}, \text{Open drain}$

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		3135		pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=100\text{ kHz}$
Output capacitance	C_{oss}		234		pF	
Reverse transfer capacitance	C_{rss}		9.2		pF	
Effective output capacitance, energy related	$C_{o(er)}$		206		pF	$V_{GS}=0\text{ V}$, $V_{DS}=0\text{ V}-240\text{ V}$
Effective output capacitance, time related	$C_{o(tr)}$		917		pF	
Turn-on delay time	$t_{d(on)}$		21.4		ns	$V_{GS}=10\text{ V}$, $V_{DS}=150\text{ V}$, $R_G=2\ \Omega$, $I_D=39\text{ A}$
Rise time	t_r		8.4		ns	
Turn-off delay time	$t_{d(off)}$		43.4		ns	
Fall time	t_f		3.6		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		54		nC	$V_{GS}=10\text{ V}$, $V_{DS}=150\text{ V}$, $I_D=39\text{ A}$
Gate-source charge	Q_{gs}		22		nC	
Gate-drain charge	Q_{gd}		20		nC	
Gate plateau voltage	$V_{plateau}$		7.6		V	

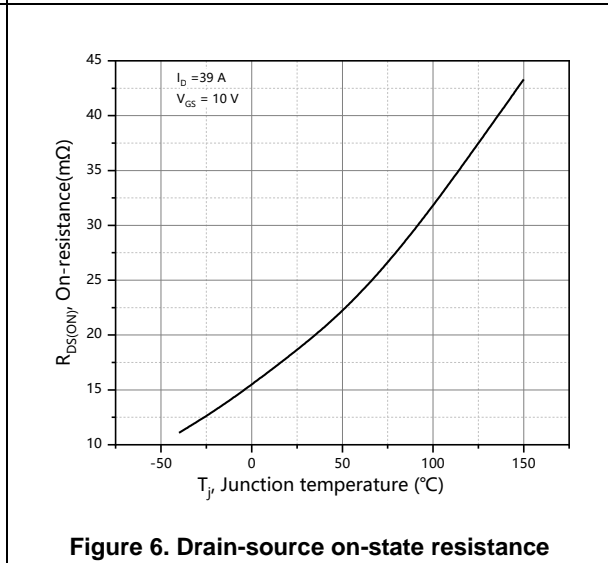
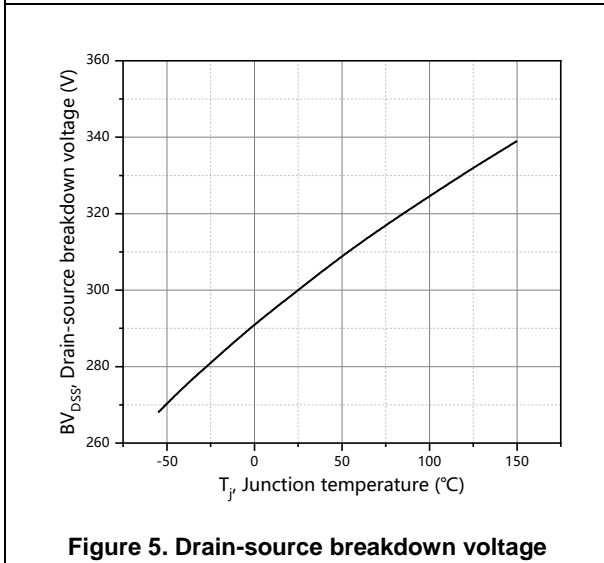
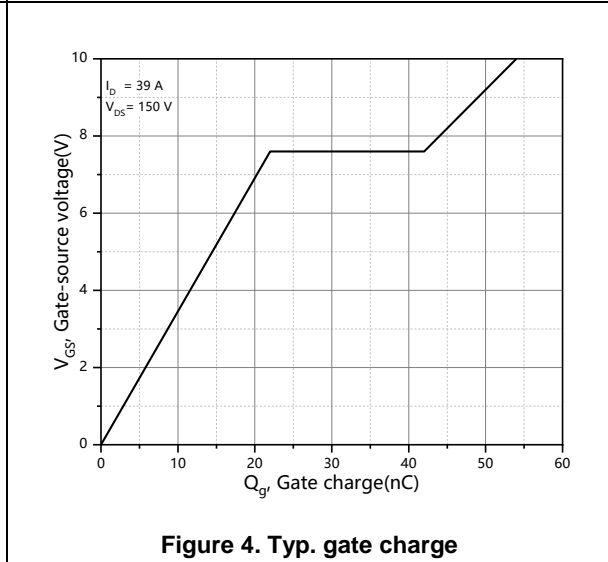
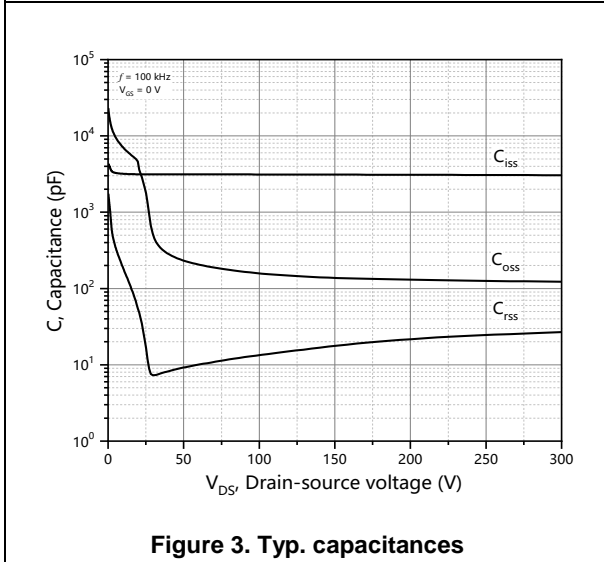
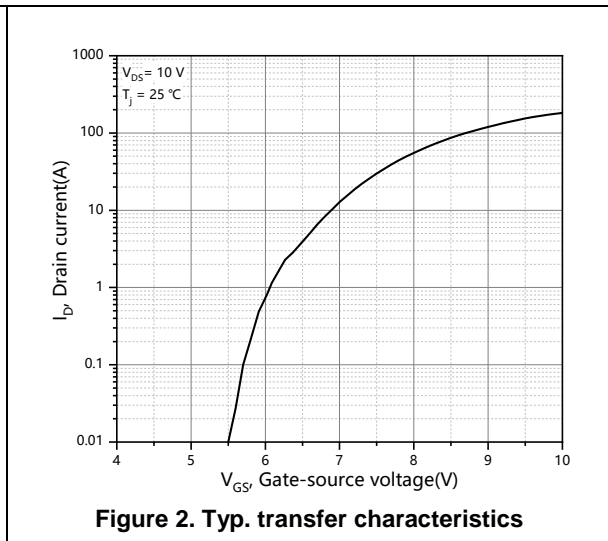
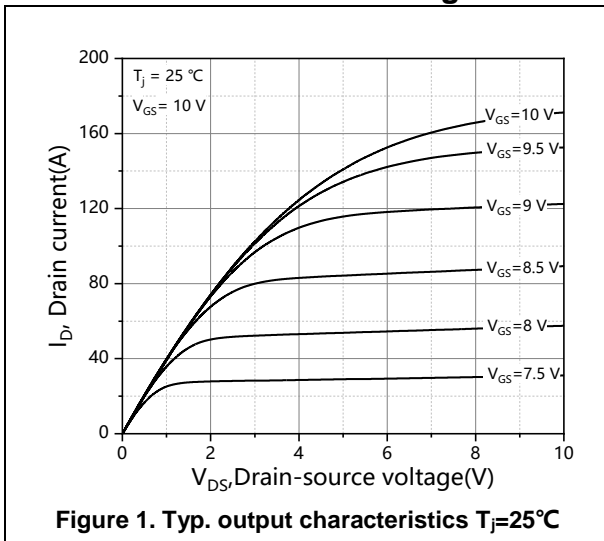
Body Diode Characteristics

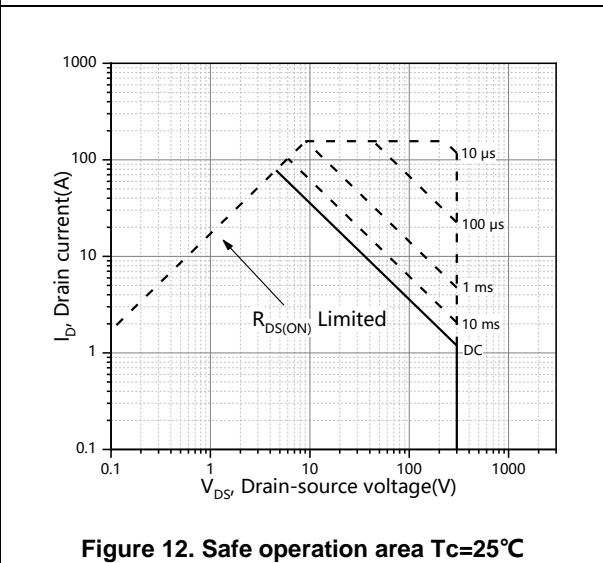
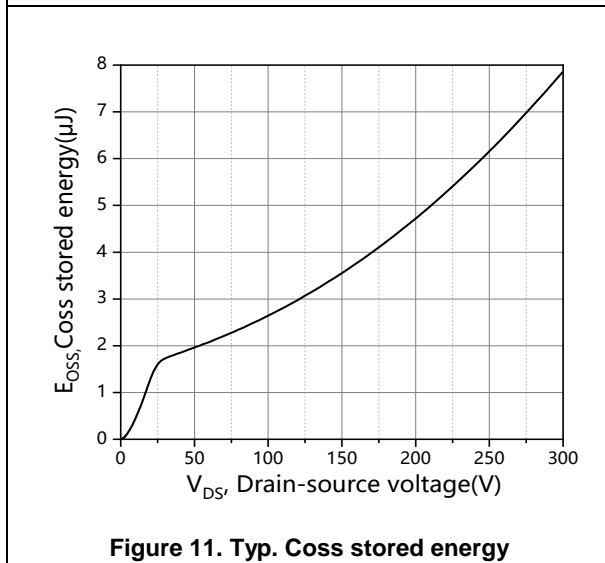
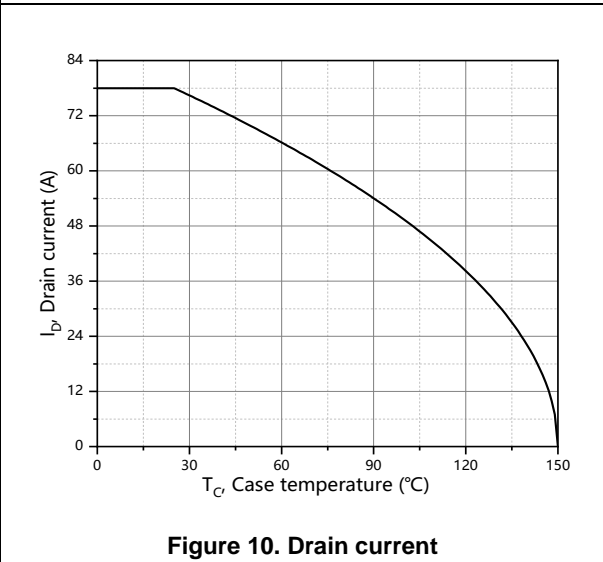
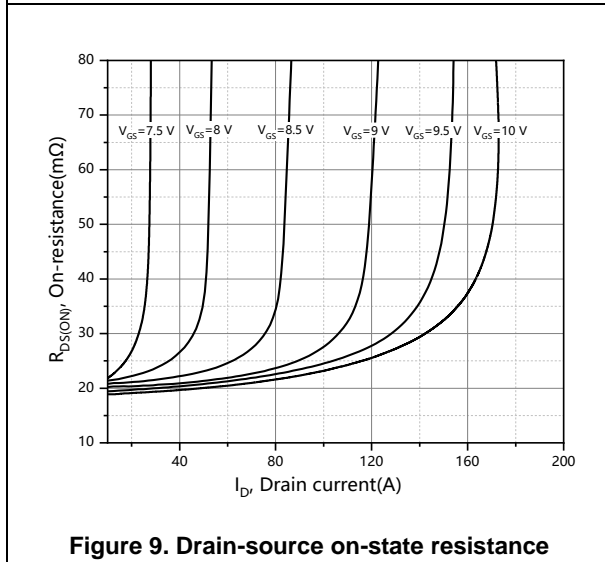
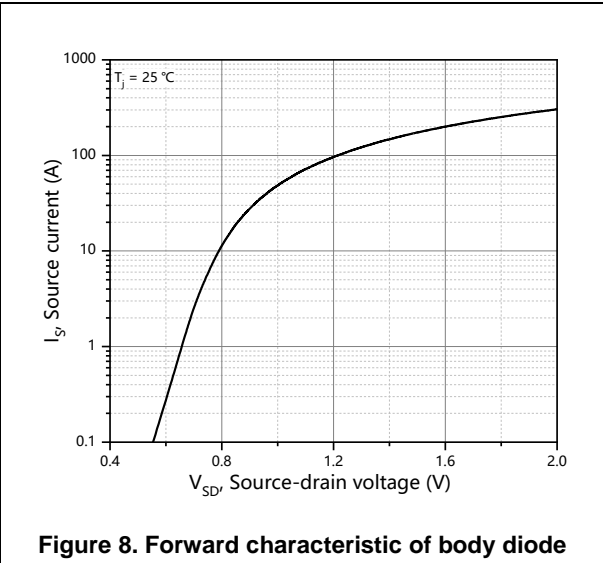
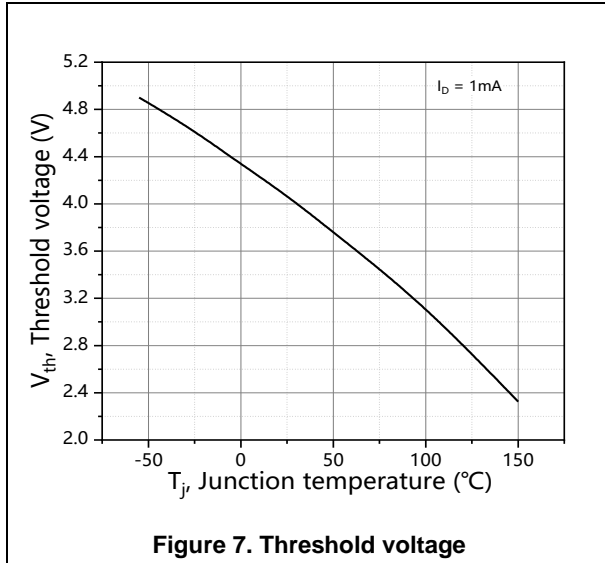
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			1.3	V	$I_S=78\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		136		ns	$V_R=150\text{ V}$, $I_S=39\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		0.53		μC	
Peak reverse recovery current	I_{rrm}		6.6		A	

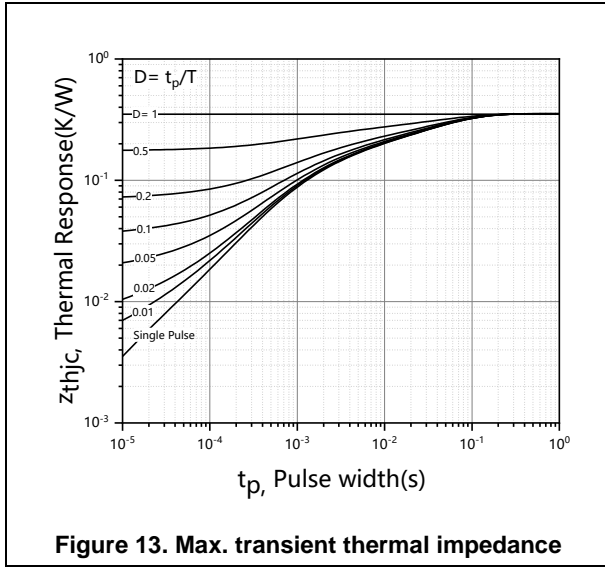
Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) $V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $L=80\text{ mH}$, starting $T_j=25\text{ }^\circ\text{C}$.

Electrical Characteristics Diagrams







Test circuits and waveforms



Figure 1. Gate charge test circuit & waveform



Figure 2. Switching time test circuit & waveforms

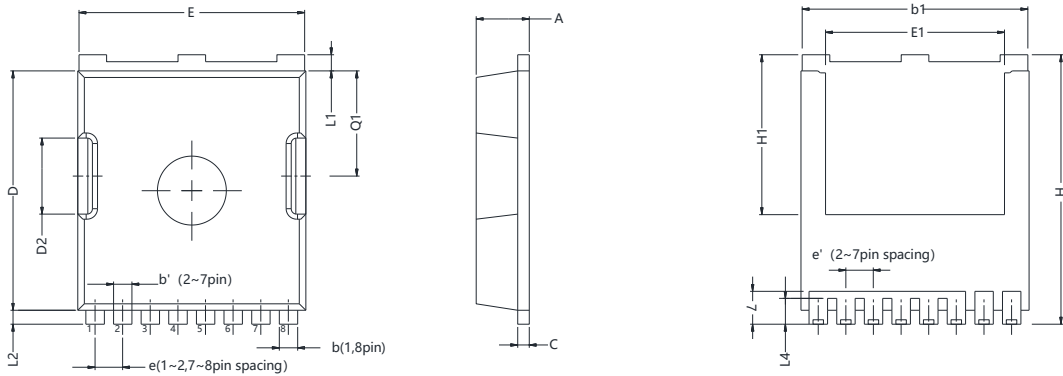


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms



Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm		
	Min	Nom	Max
A	2.15	2.30	2.45
b	0.75	0.75	0.85
b'	0.70	0.70	0.80
b1	9.65	9.80	9.95
C	0.45	0.50	0.60
D	10.18	10.38	10.58
D2	3.15	3.30	3.45
E	9.70	9.90	10.10
E1	7.95	8.10	8.25
e	BSC 1.225		
e'	BSC 1.20		
Q1	4.40	4.55	4.70
H	11.48	11.68	11.88
H1	6.80	6.95	7.10
L	1.60	1.80	2.00
L1	0.50	0.70	0.90
L2	0.48	0.60	0.72
L4	1.00	1.15	1.30

Version: TOLL-P package outline dimension

Ordering Information

Package Type	Units/ Reel	Reels/ Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
TOLL-P	1200	1	1200	5	6000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
OSG30R025TF	TOLL	yes	yes	yes

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Oriental Semiconductor hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

For further information on technology, delivery terms and conditions and prices, please contact the Oriental Semiconductor sales representatives (www.orientalsemi.com).

© Oriental Semiconductor Co.,Ltd. All Rights Reserved /

Revision History

Version	Revision History	Date
V1.0	Initial release	2025-07-30