General Description

FSMOS® MOSFET is based on Oriental Semiconductor's unique device design to achieve low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The low V_{th} series is specially optimized for synchronous rectification systems with low driving voltage.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent reliability and uniformity
- Fast switching and soft recovery

RoHS compliant

Applications

- PD charger
- Motor driver
- Switching voltage regulator
- DC-DC convertor
- Switching mode power supply

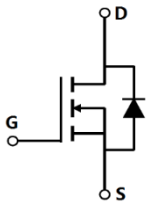
Key Performance Parameters

Parameter	Value	Unit
V_{DS}	65	V
$I_{D,\ pulse}$	48	A
$R_{DS(ON),\ max}$ @ V_{GS}=10V	11	mΩ
Q_g	18.4	nC
PD	4	W

Marking Information

Product Name	Package	Marking
SFS06R10BF	SOP8	SFS06R10B

Package & Pin information



Absolute Maximum Ratings at T_j=25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	65	V
Gate-source voltage	V_{GS}	±20	V
Continuous drain current[1], T_C=25 °C	I_D	12	A
Pulsed drain current[2], T_C=25 °C	$I_{D,\ pulse}$	48	A
Continuous diode forward current[1], T_C=25 °C	I_S	12	A
Diode pulsed current[2], T_C=25 °C	$I_{S,\ pulse}$	48	A
Power dissipation[3], T_C=25 °C	P_D	4	W
Single pulsed avalanche energy[4]	E_{AS}	30	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-ambient	$R_{\theta JA}$	62	°C/W

Electrical Characteristics at T_j=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	65			V	V_{GS}=0 V, I_D=250 μA
Gate threshold voltage	$V_{GS(th)}$	1.5		2.5	V	V_{DS}=V_{GS}, I_D=250 μA
Drain-source on-state resistance	$R_{DS(ON)}$		9	11	mΩ	V_{GS}=10 V, I_D=20 A
Drain-source on-state resistance	$R_{DS(ON)}$		11	14	mΩ	V_{GS}=4.5 V, I_D=10 A
Gate-source leakage current	I_{GSS}			100	nA	V_{GS}=20 V
				-100		V_{GS}=-20 V
Drain-source leakage current	I_{DSS}			1	μA	V_{DS}=60 V, V_{GS}=0 V

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		1182		pF	V_{GS}=0 V, V_{DS}=50 V, f=100 kHz
Output capacitance	C_{oss}		199		pF	
Reverse transfer capacitance	C_{rss}		4.1		pF	
Turn-on delay time	$t_{d(on)}$		17.9		ns	V_{GS}=10 V, V_{DS}=50 V, R_G=2 Ω, I_D=10 A
Rise time	t_r		4.0		ns	
Turn-off delay time	$t_{d(off)}$		34.9		ns	
Fall time	t_f		5.5		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		18.4		nC	V_{GS}=10 V, V_{DS}=50 V, I_D=10 A
Gate-source charge	Q_{gs}		3.3		nC	
Gate-drain charge	Q_{gd}		3.1		nC	
Gate plateau voltage	$V_{plateau}$		2.8		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			1.3	V	I_S=20 A, V_{GS}=0 V
Reverse recovery time	t_{rr}		41.8		ns	V_R=50 V, I_S=10 A, di/dt=100 A/μs
Reverse recovery charge	Q_{rr}		36.1		nC	
Peak reverse recovery current	I_{rrm}		1.4		A	

Note

1) Calculated continuous current based on maximum allowable junction temperature.
2) Repetitive rating; pulse width limited by max. junction temperature.
3) Pd is based on max. junction temperature, using junction-case thermal resistance.
4) V_{DD}=50 V,V_{GS}=10 V, L=0.3 mH, starting T_j=25 °C.

Electrical Characteristics Diagrams

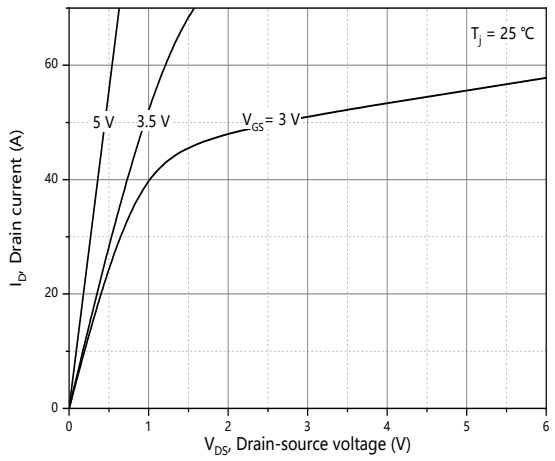


Figure 1. Typ. output characteristics

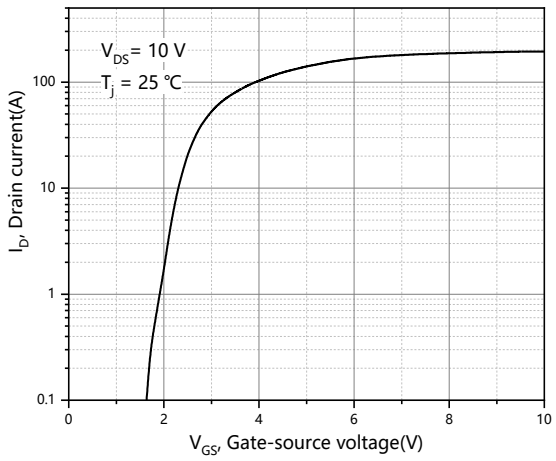


Figure 2. Typ. transfer characteristics

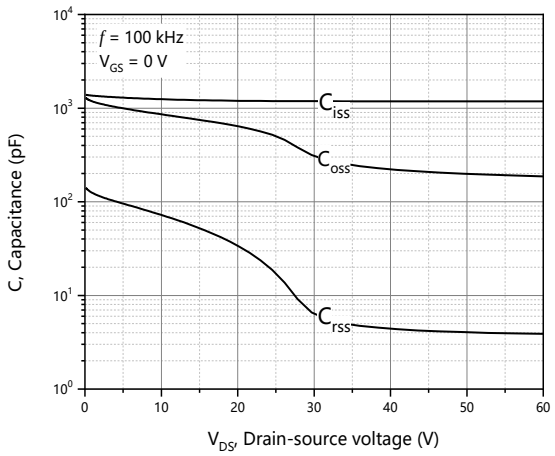


Figure 3. Typ. capacitances

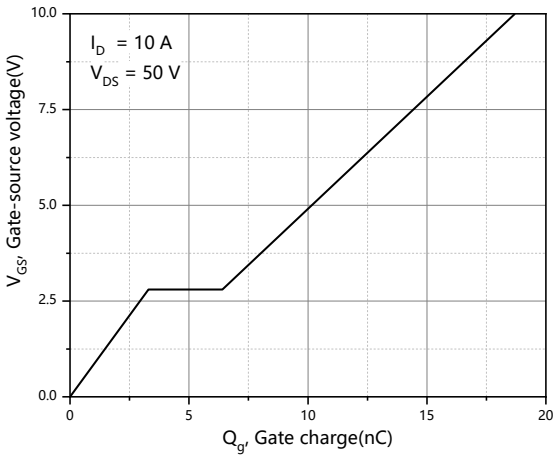


Figure 4. Typ. gate charge

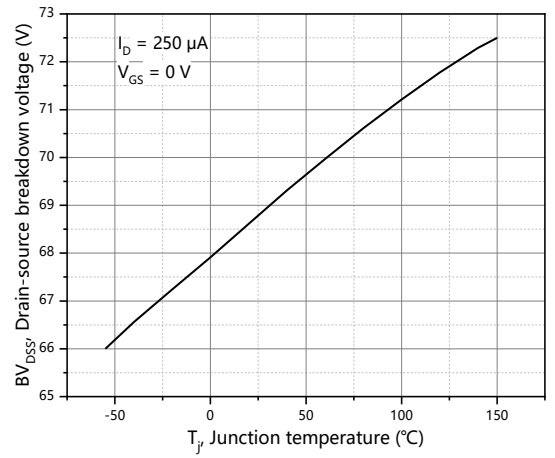


Figure 5. Drain-source breakdown voltage

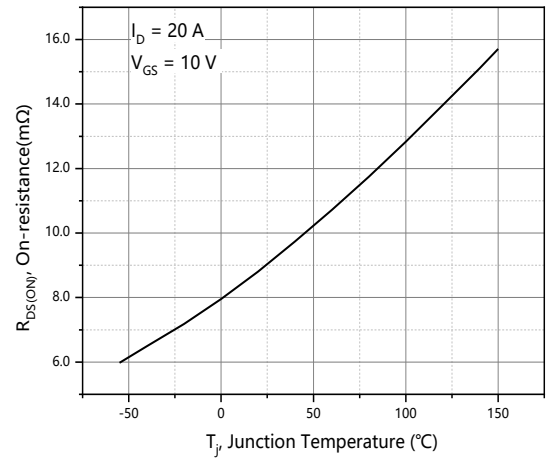


Figure 6. Drain-source on-state resistance

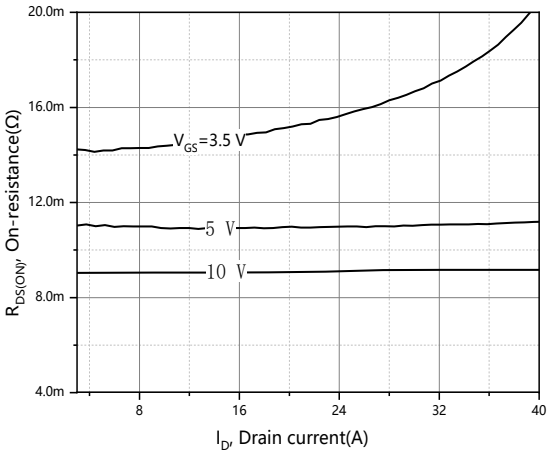


Figure 7. Drain-source on-state resistance

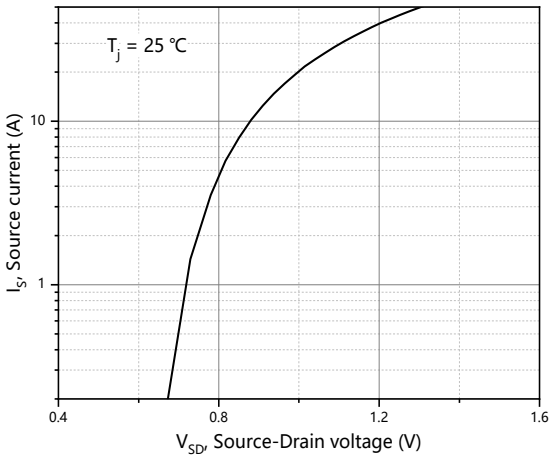


Figure 8. Forward characteristic of body diode

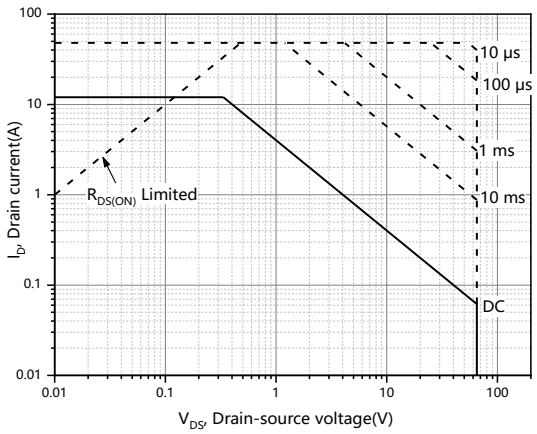


Figure 9. Safe operation area T_C=25 ℃

Test circuits and waveforms

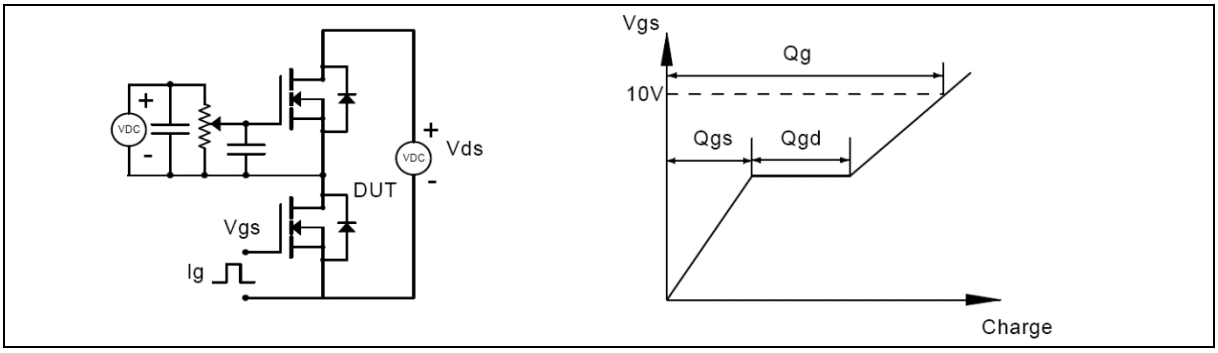


Figure 1. Gate charge test circuit & waveform

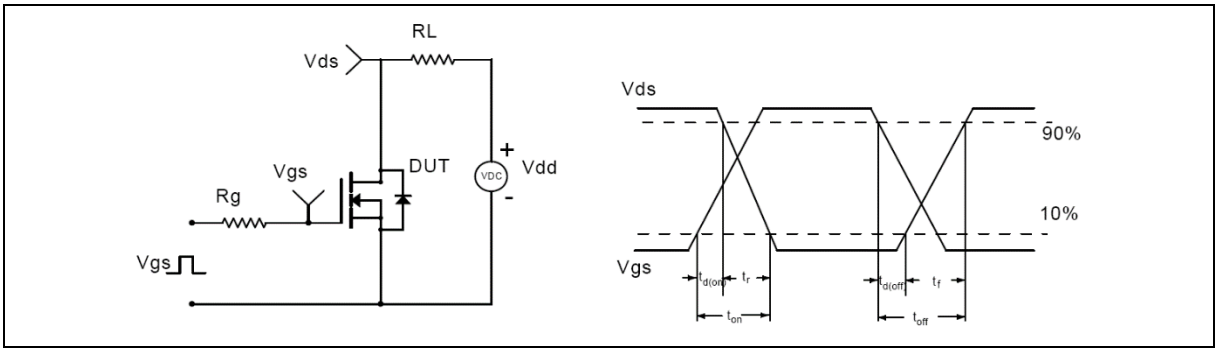


Figure 2. Switching time test circuit & waveforms

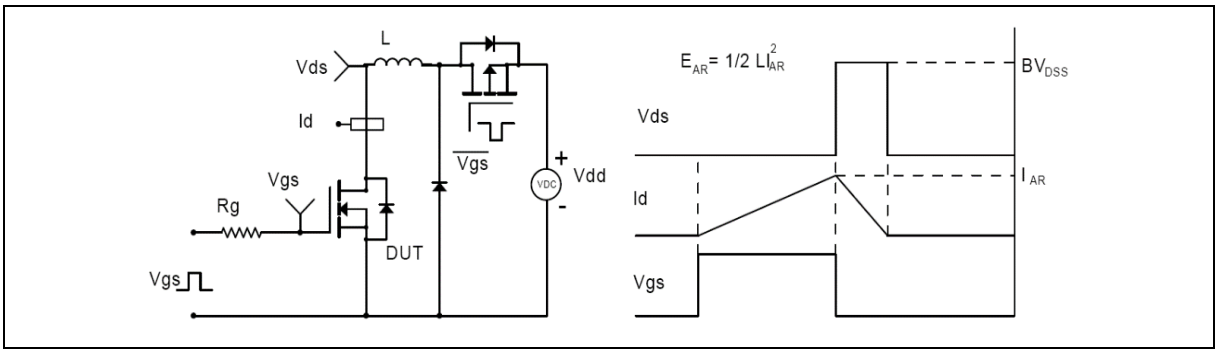


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

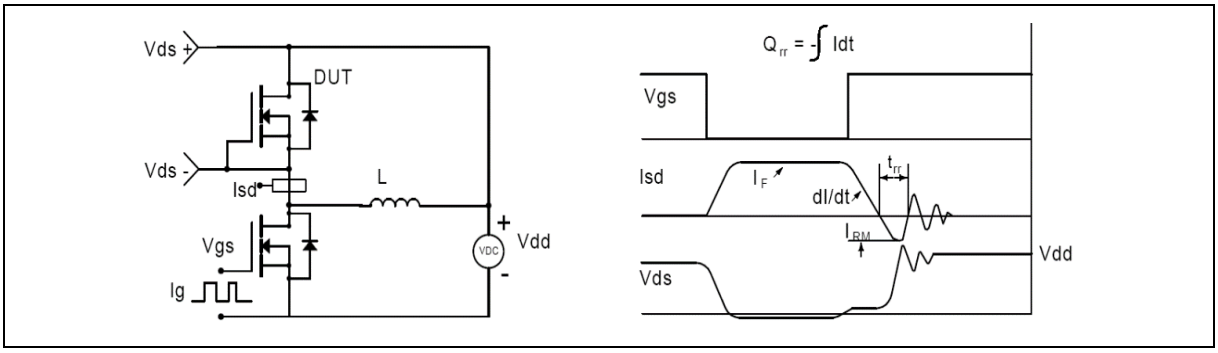
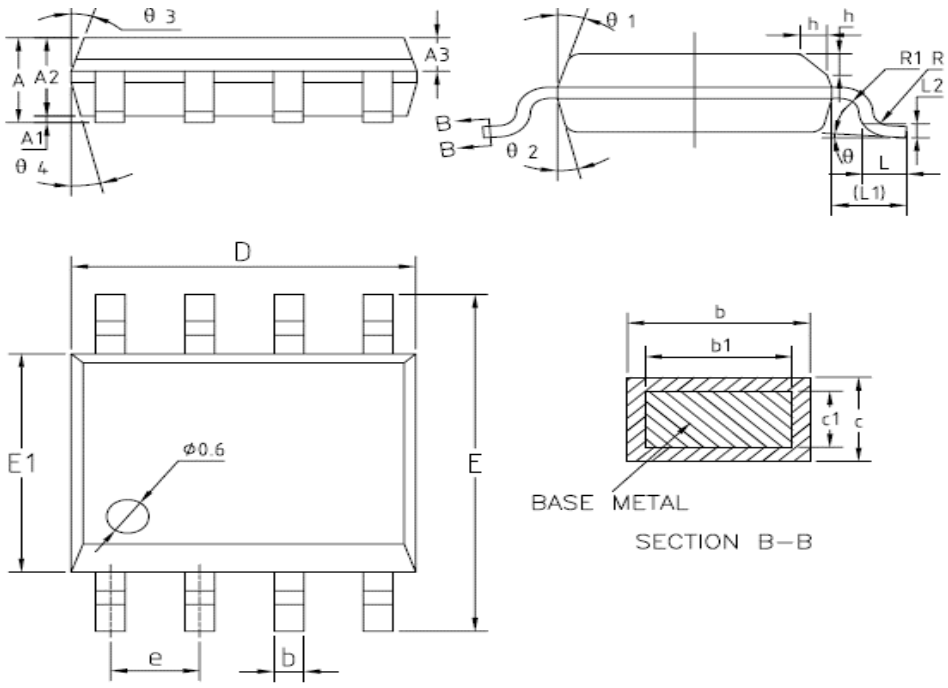


Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm		
	Min	Nom	Max
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	-	0.51
L1	1.04 REF		
L2	0.25 BSC		
b1	0.37	0.42	0.47
c	0.18	-	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
R	0.07	-	-
R1	0.07	-	-
h	0.30	0.40	0.50
θ	0°	-	8°
θ1	15°	17°	19°
θ2	11°	13°	15°
θ3	15°	17°	19°
θ4	11°	13°	15°

Version 1: SOP8-K package outline dimension

Ordering Information

Package Type	Units/ Reel	Reels / Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
SOP8-K	2500	2	5000	6	30000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
SFS06R10BF	SOP8	yes	yes	yes

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