General Description

FSMOS® MOSFET is based on Oriental Semiconductor's unique device design to achieve low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The low V_{th} series is specially optimized for synchronous rectification systems with low driving voltage.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent reliability and uniformity
- Fast switching and soft recovery

RoHS compliant

Applications

- Switching mode power supply
- Motor driver
- Battery protection
- DC-DC convertor
- Inverters
- UPS

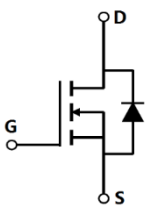
Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
$I_{D,\ pulse}$	200	A
$R_{DS(ON)\ max}$ @ V_{GS}=10V	10	mΩ
Q_g	22	nC

Marking Information

Product Name	Package	Marking
SFS08R10DAF	TO252	SFS08R10DA

Package & Pin information



Absolute Maximum Ratings at T_j=25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	80	V
Gate source voltage	V_{GS}	±20	V
Continuous drain current[1], T_C=25 °C	I_D	50	A
Pulsed drain current[2], T_C=25 °C	$I_{D,\ pulse}$	200	A
Continuous diode forward current[1], T_C=25 °C	I_S	50	A
Diode pulsed current[2], T_C=25 °C	$I_{S,\ Pulse}$	200	A
Power dissipation[3], T_C=25 °C	P_D	66	W
Single pulsed avalanche energy[5]	E_{AS}	54	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	2.27	°C/W
Thermal resistance, junction-ambient[4]	$R_{\theta JA}$	62	°C/W

Electrical Characteristics at T_j=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	80			V	V_{GS}=0 V, I_D=250 μA
Gate threshold voltage	$V_{GS(th)}$	1.0		2.5	V	V_{DS}=V_{GS}, I_D=250 μA
Drain-source on-state resistance	$R_{DS(ON)}$		7.0	10	mΩ	V_{GS}=10 V, I_D=20 A
Drain-source on-state resistance	$R_{DS(ON)}$		9.1	13	mΩ	V_{GS}=4.5 V, I_D=20 A
Gate-source leakage current	I_{GSS}			100	nA	V_{GS}=20 V
				-100		V_{GS}=-20 V
Drain-source leakage current	I_{DSS}			1	μA	V_{DS}=80 V, V_{GS}=0 V
Gate resistance	R_G		2.5		Ω	f=1 MHz, Open drain

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		1350		pF	V_{GS}=0 V, V_{DS}=25 V, f=100 kHz
Output capacitance	C_{oss}		571		pF	
Reverse transfer capacitance	C_{rss}		51		pF	
Turn-on delay time	$t_{d(on)}$		7.2		ns	V_{GS}=10 V, V_{DS}=40 V, R_G=2 Ω, I_D=20 A
Rise time	t_r		5		ns	
Turn-off delay time	$t_{d(off)}$		23.5		ns	
Fall time	t_f		6		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		22		nC	V_{GS}=10 V, V_{DS}=40 V, I_D=20 A
Gate-source charge	Q_{gs}		3		nC	
Gate-drain charge	Q_{gd}		5		nC	
Gate plateau voltage	$V_{plateau}$		3.8		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			1.3	V	I_S=12 A, V_{GS}=0 V
Reverse recovery time	t_{rr}		38.5		ns	V_R=40 V, I_S=20 A, di/dt=100 A/μs
Reverse recovery charge	Q_{rr}		40.3		nC	
Peak reverse recovery current	I_{rrm}		1.9		A	

Note

1) Calculated continuous current based on maximum allowable junction temperature.
2) Repetitive rating; pulse width limited by max. junction temperature.
3) Pd is based on max. junction temperature, using junction-case thermal resistance.
4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 °C.
5) V_{DD}=50 V,V_{GS}=10 V, L=0.3 mH, starting T_j=25 °C.

Electrical Characteristics Diagrams

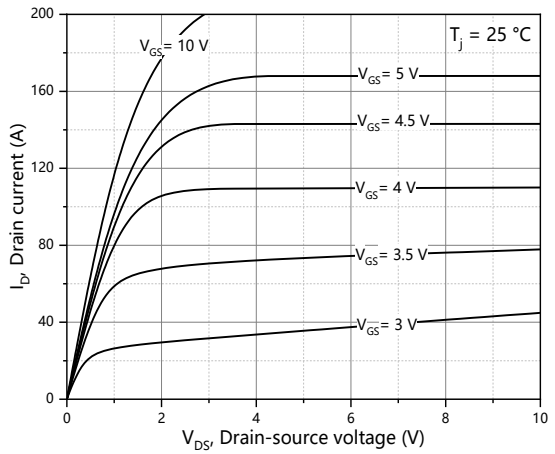


Figure 1. Typ. output characteristics

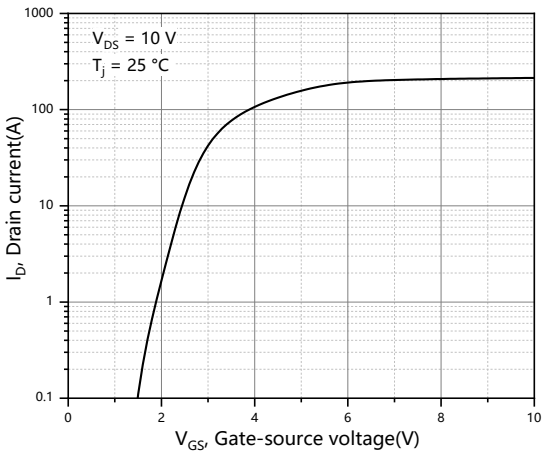


Figure 2. Typ. transfer characteristics

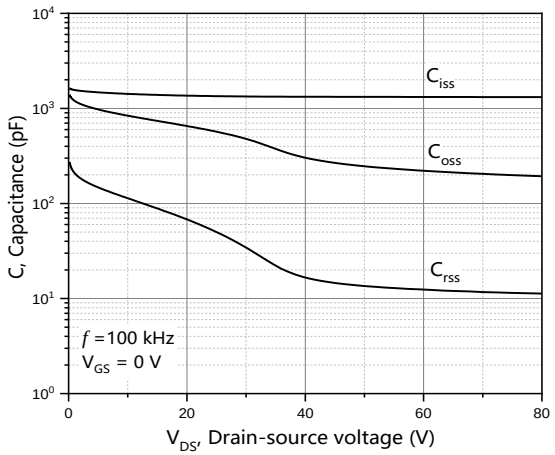


Figure 3. Typ. capacitances

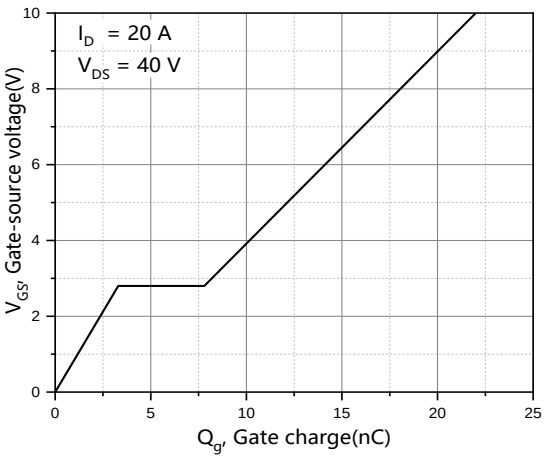


Figure 4. Typ. gate charge

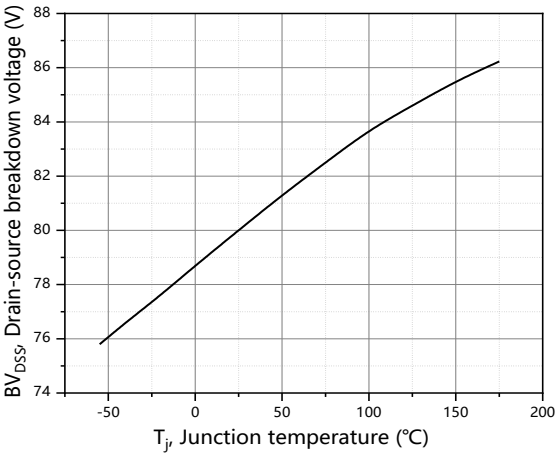


Figure 5. Drain-source breakdown voltage

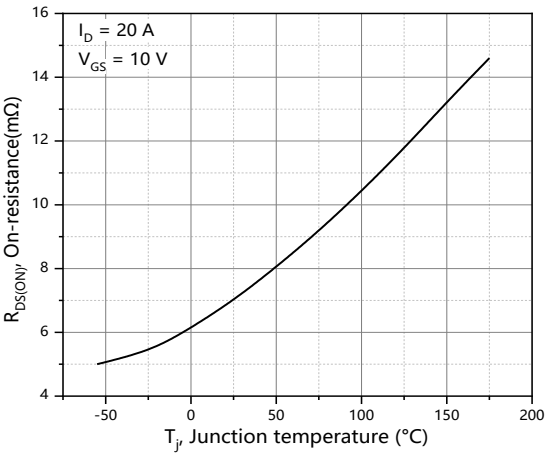


Figure 6. Drain-source on-state resistance

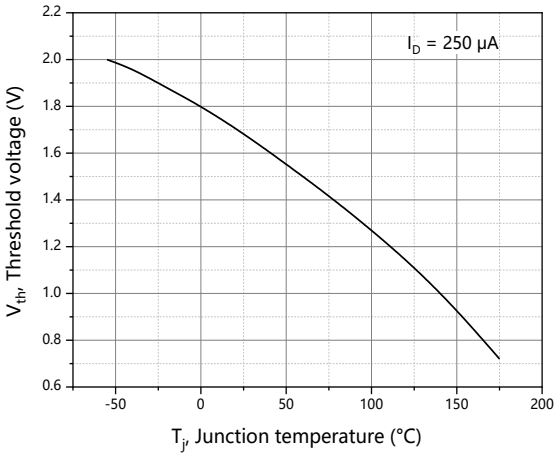


Figure 7. Threshold voltage

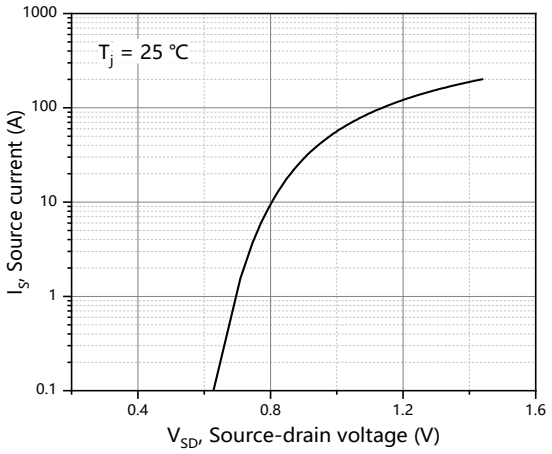


Figure 8. Forward characteristic of body diode

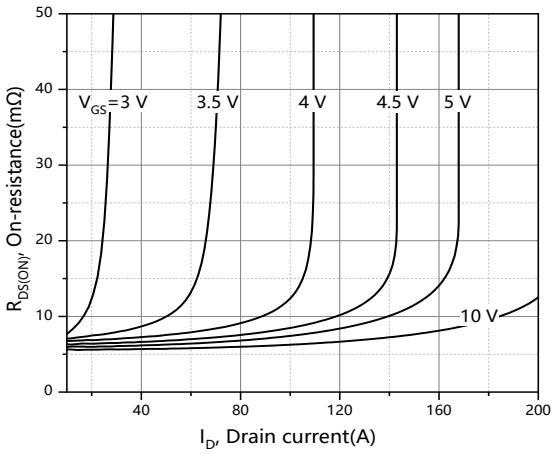


Figure 9. Drain-source on-state resistance

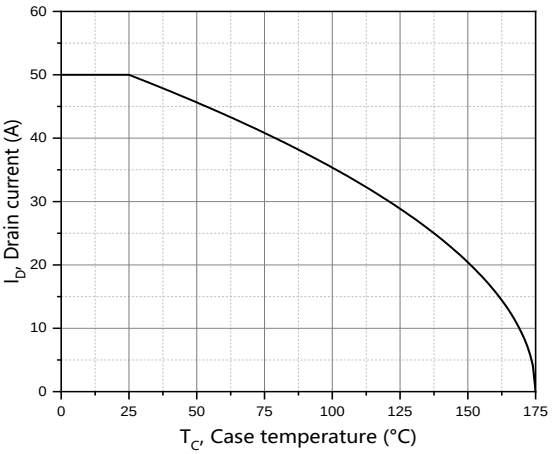


Figure 10. Drain current

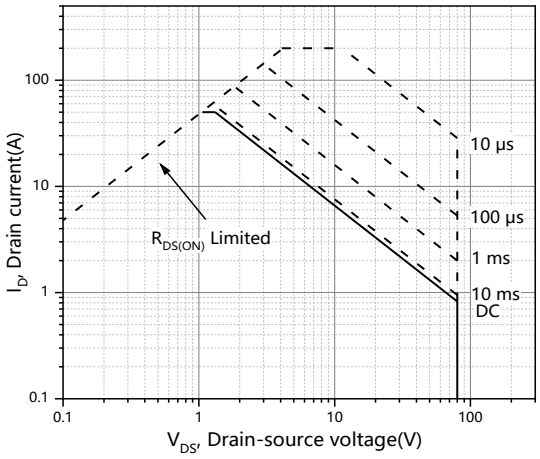


Figure 11. Safe operation area T_C=25 °C

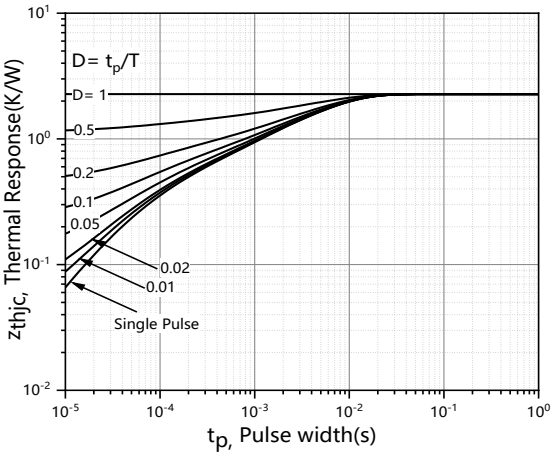


Figure 12. Max transient thermal impedance

Test circuits and waveforms

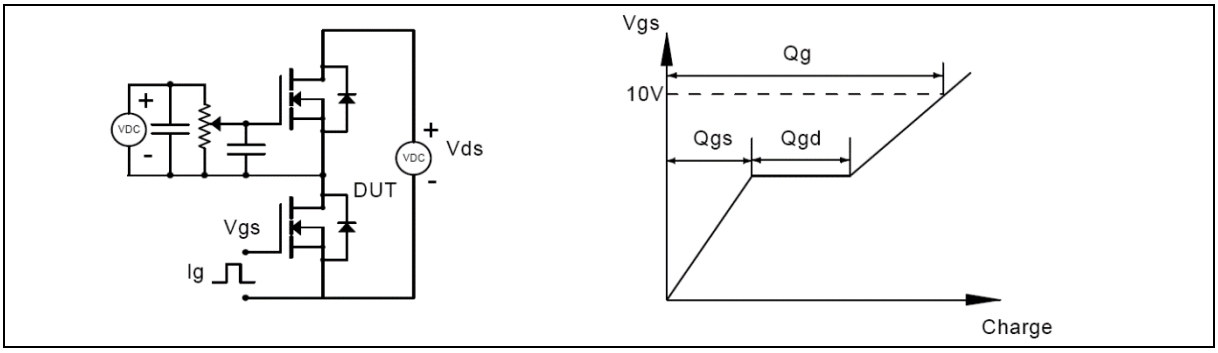


Figure 1. Gate charge test circuit & waveform

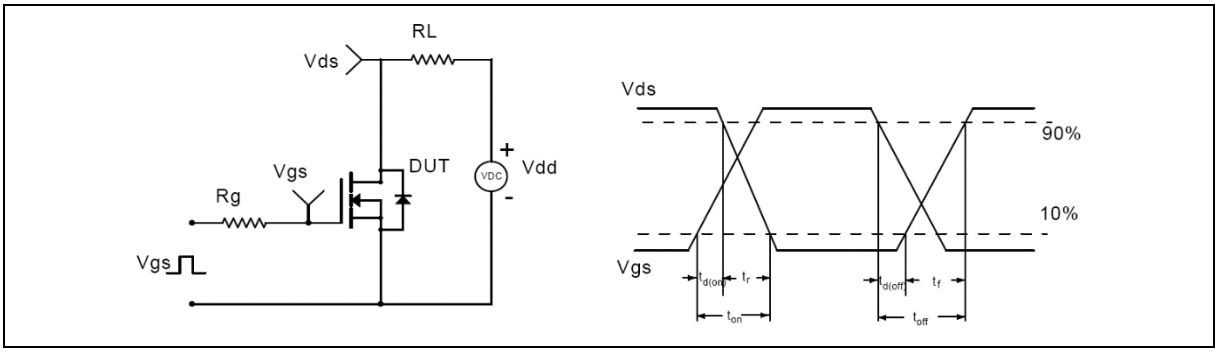


Figure 2. Switching time test circuit & waveforms

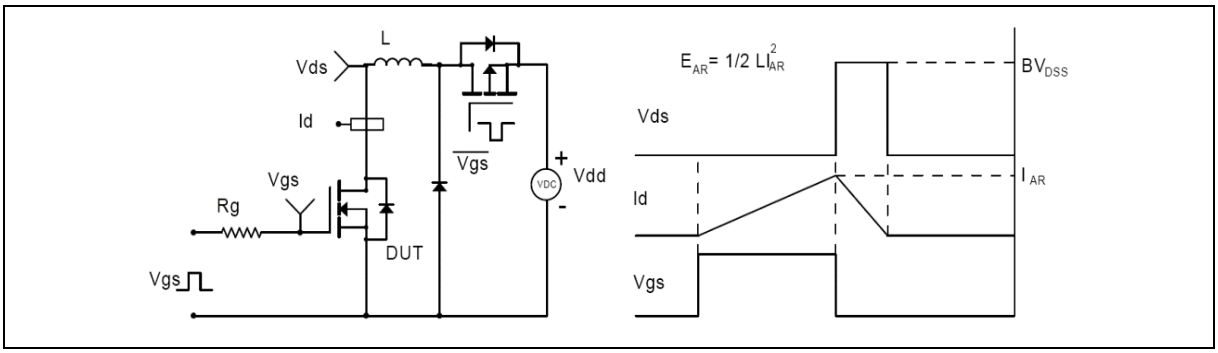


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

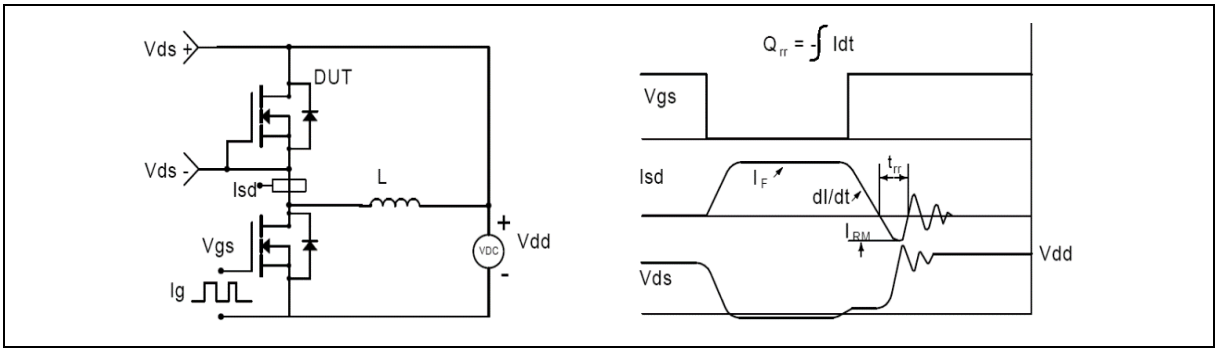
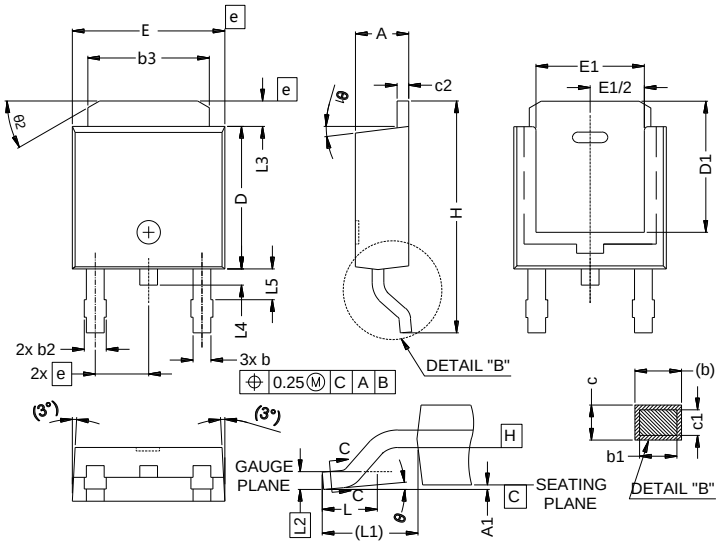


Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm	
	Min	Max
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34
L	1.50	1.78
L1	2.74 REF	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Version : TO252-S package outline dimension

Ordering Information

Package Type	Units/ Reel	Reels / Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
TO252-S	2500	1	2500	10	25000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
SFS08R10DAF	TO252	yes	yes	yes

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Oriental Semiconductor hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

For further information on technology, delivery terms and conditions and prices, please contact the Oriental Semiconductor sales representatives (www.orientalsemi.com).

Revision History

Version	Revision History	Date
V1.0	Initial release	2023-09-01
V1.1	Update Marking	2025-09-19

ORIENTAL SEMICONDUCTOR

A Power Semiconductor Innovator