

General Description

FSMOS[®] MOSFET is based on Oriental Semiconductor's unique device design to achieve low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The low V_{th} series is specially optimized for synchronous rectification systems with low driving voltage.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent reliability and uniformity
- Fast switching and soft recovery



Applications

- PD charger
- Motor driver
- Switching voltage regulator
- DC-DC convertor
- Switching mode power supply

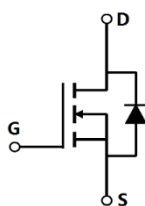
Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
I_D , pulse	30	A
$R_{DS(ON), max}$ @ $V_{GS}=10V$	20	m Ω
Q_g	14	nC
PD	2.5	W

Marking Information

Product Name	Package	Marking
SFS10R20BF	SOP8	SFS10R20B

Package & Pin information



Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	7.5	A
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D, pulse}$	30	A
Continuous diode forward current ¹⁾ , $T_C=25^\circ\text{C}$	I_S	7.5	A
Diode pulsed current ²⁾ , $T_C=25^\circ\text{C}$	$I_{S, pulse}$	30	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	2.5	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	18	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Electrical Characteristics at $T_j=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	100			V	$V_{GS}=0\text{ V}, I_D=250\ \mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1		2.5	V	$V_{DS}=V_{GS}, I_D=250\ \mu\text{A}$
Drain-source on-state resistance	$R_{DS(ON)}$		16	20	m Ω	$V_{GS}=10\text{ V}, I_D=30\text{ A}$
Drain-source on-state resistance	$R_{DS(ON)}$		20	24	m Ω	$V_{GS}=4.5\text{ V}, I_D=30\text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=100\text{ V}, V_{GS}=0\text{ V}$
Gate resistance	R_G		2.1		Ω	$f=1\text{ MHz}, \text{Open drain}$

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		967		pF	$V_{GS}=0\text{ V}$, $V_{DS}=25\text{ V}$, $f=100\text{ kHz}$
Output capacitance	C_{oss}		493		pF	
Reverse transfer capacitance	C_{rss}		31		pF	
Turn-on delay time	$t_{d(on)}$		8		ns	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_G=2\ \Omega$, $I_D=25\text{ A}$
Rise time	t_r		3		ns	
Turn-off delay time	$t_{d(off)}$		16		ns	
Fall time	t_f		2.4		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		14		nC	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $I_D=25\text{ A}$
Gate-source charge	Q_{gs}		3		nC	
Gate-drain charge	Q_{gd}		2.5		nC	
Gate plateau voltage	$V_{plateau}$		3.4		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			1.3	V	$I_S=30\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		54		ns	$V_R=50\text{ V}$, $I_S=25\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		51		nC	
Peak reverse recovery current	I_{rrm}		1.9		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^\circ\text{C}$.
- 5) $V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $L=0.3\text{ mH}$, starting $T_j=25\text{ }^\circ\text{C}$.

Electrical Characteristics Diagrams

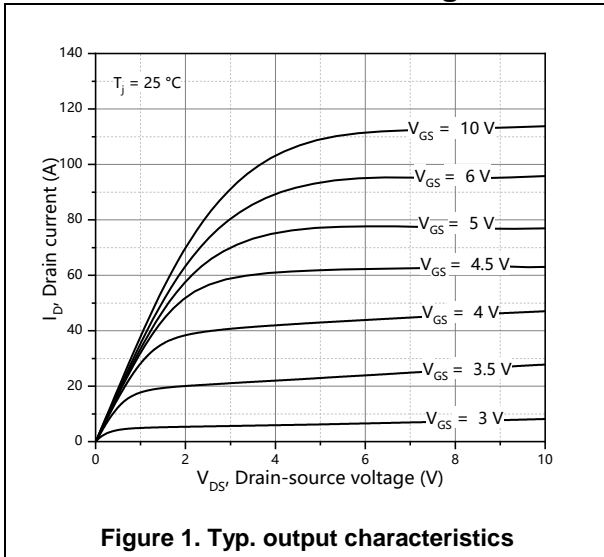


Figure 1. Typ. output characteristics

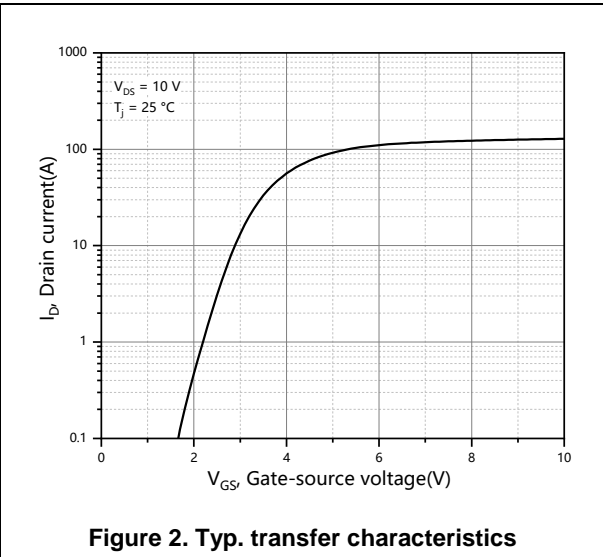


Figure 2. Typ. transfer characteristics

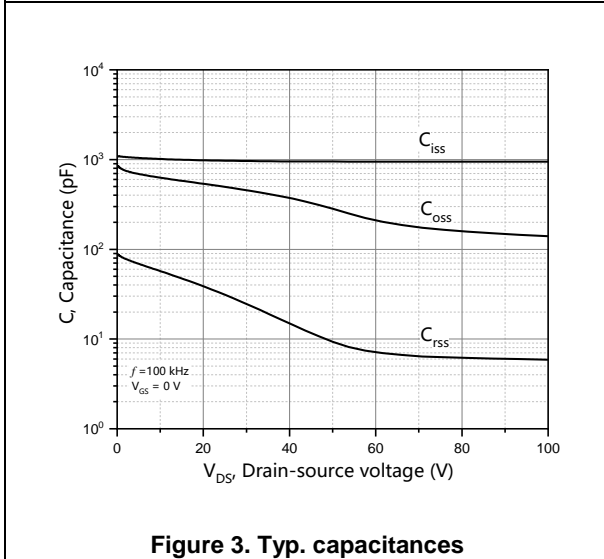


Figure 3. Typ. capacitances

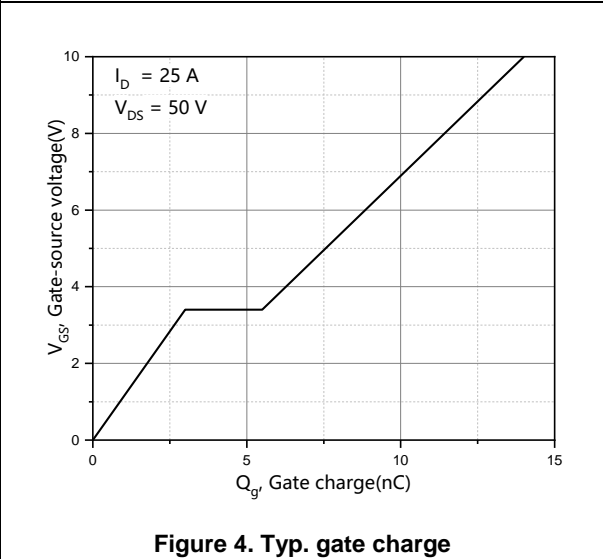


Figure 4. Typ. gate charge

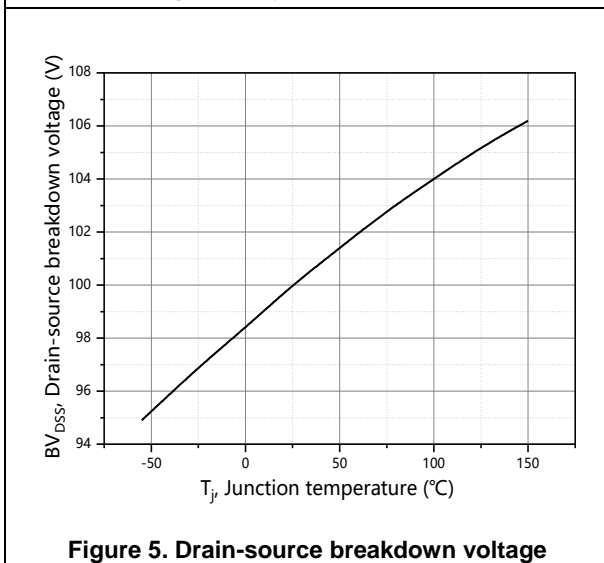


Figure 5. Drain-source breakdown voltage

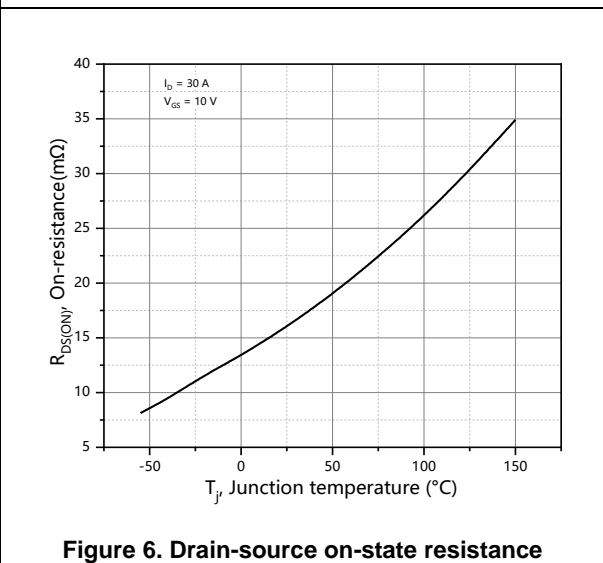
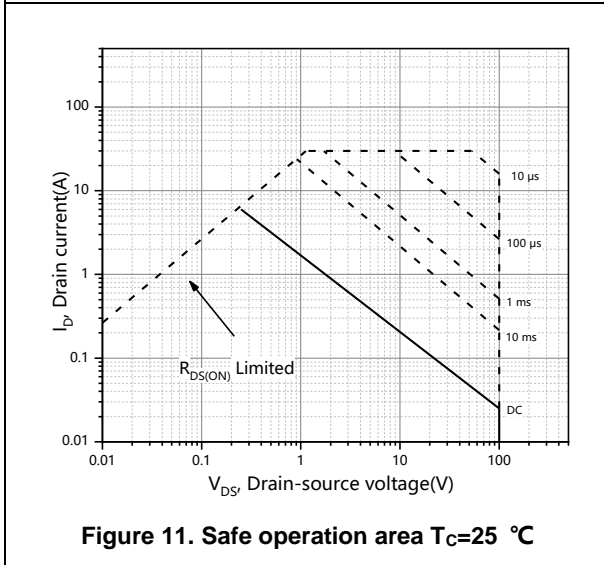
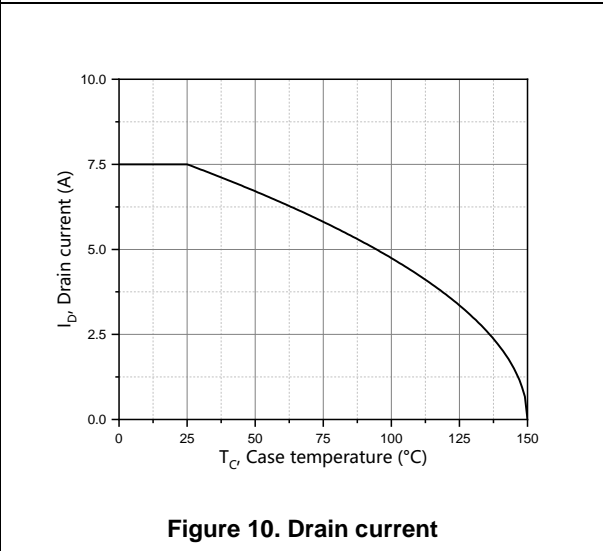
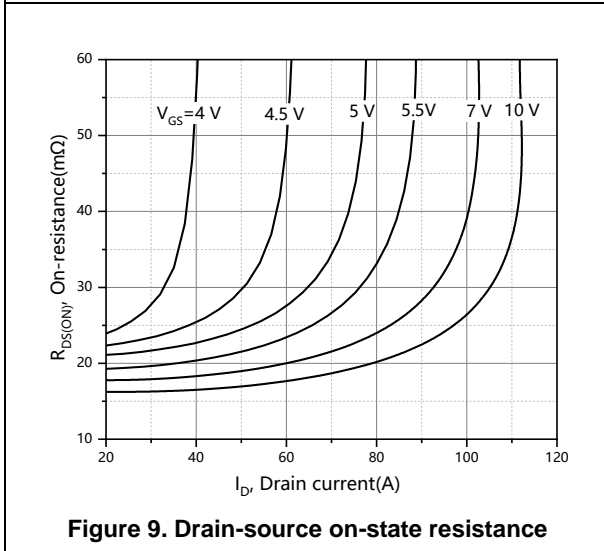
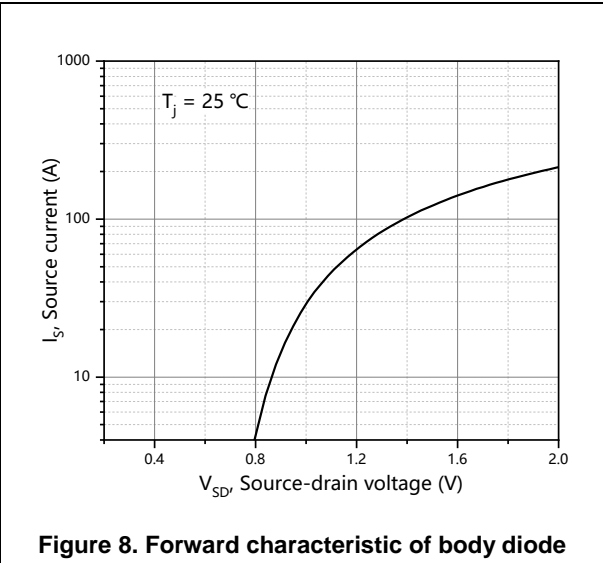
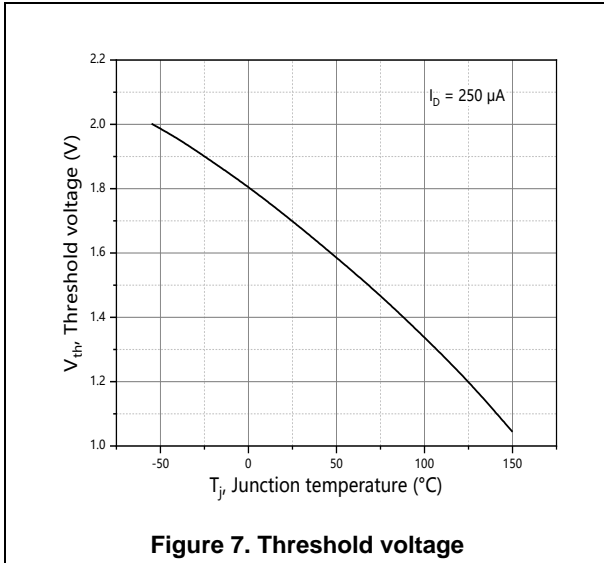


Figure 6. Drain-source on-state resistance



Test circuits and waveforms



Figure 1. Gate charge test circuit & waveform



Figure 2. Switching time test circuit & waveforms

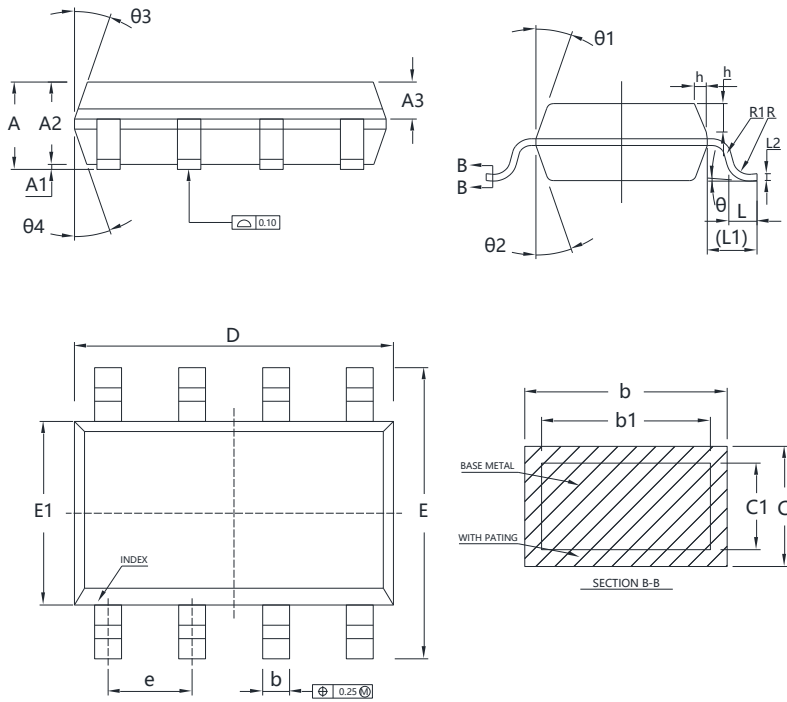


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms



Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm		
	Min	Nom	Max
A	1.45	1.55	1.65
A1	0.10	0.15	0.20
A2	1.353	1.40	1.453
A3	0.55	0.60	0.65
b	0.38	-	0.51
b1	0.37	0.42	0.47
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.85	4.90	4.95
E	5.85	6.00	6.15
E1	3.85	3.90	3.95
e	1.245	1.270	1.295
h	0.30	0.40	0.50
L	0.45	0.60	0.75
L1	-	1.04 REF	-
L2	-	0.25 BSC	-

Version: SOP8-G package outline dimension

Ordering Information

Package Type	Units/ Reel	Reels/ Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
SOP8-G	4000	2	8000	6	48000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
SFS10R20BF	SOP8	yes	yes	yes

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Oriental Semiconductor hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

For further information on technology, delivery terms and conditions and prices, please contact the Oriental Semiconductor sales representatives (www.orientalsemi.com).

© Oriental Semiconductor Co.,Ltd. All Rights Reserved 

Revision History

Version	Revision History	Date
V1.0	Initial release	2024-12-01