

General Description

FSMOS[®] MOSFET is based on Oriental Semiconductor's unique device design to achieve low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The high V_{th} series is specially designed to use in motor control systems with driving voltage of more than 10V.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent reliability and uniformity
- Fast switching and soft recovery



Applications

- PD charger
- Motor driver
- Switching voltage regulator
- DC-DC convertor
- Switching mode power supply

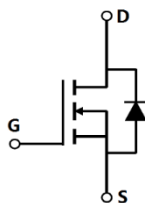
Key Performance Parameters

Parameter	Value	Unit
V_{DS}	200	V
I_D , pulse	236	A
$R_{DS(ON)}$, max @ $V_{GS}=10V$	20	m Ω
Q_g	30	nC

Marking Information

Product Name	Package	Marking
SFS20R20GNF	PDFN5*6	SFS20R20GN

Package & Pin information



Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	200	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	59	A
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D, pulse}$	236	A
Continuous diode forward current ¹⁾ , $T_C=25^\circ\text{C}$	I_S	59	A
Diode pulsed current ²⁾ , $T_C=25^\circ\text{C}$	$I_{S, pulse}$	236	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	185	W
Single pulsed avalanche energy ⁴⁾	E_{AS}	108	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.81	$^\circ\text{C/W}$
Thermal resistance, junction-ambient	$R_{\theta JA}$	62	$^\circ\text{C/W}$

Electrical Characteristics at $T_j=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	200			V	$V_{GS}=0\text{ V}, I_D=250\ \mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	2.5		4.5	V	$V_{DS}=V_{GS}, I_D=250\ \mu\text{A}$
Drain-source on-state resistance	$R_{DS(ON)}$		15.4	20	m Ω	$V_{GS}=10\text{ V}, I_D=30\text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=160\text{ V}, V_{GS}=0\text{ V}$
Gate resistance	R_G		2.4		Ω	$f=1\text{ MHz}, \text{Open drain}$

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		1938		pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=100\text{ kHz}$
Output capacitance	C_{oss}		280		pF	
Reverse transfer capacitance	C_{rss}		8.2		pF	
Turn-on delay time	$t_{d(on)}$		16		ns	$V_{GS}=10\text{ V}$, $V_{DS}=100\text{ V}$, $R_G=2\ \Omega$, $I_D=30\text{ A}$
Rise time	t_r		10		ns	
Turn-off delay time	$t_{d(off)}$		21		ns	
Fall time	t_f		8.8		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		30		nC	$V_{GS}=10\text{ V}$, $V_{DS}=100\text{ V}$, $I_D=30\text{ A}$
Gate-source charge	Q_{gs}		13		nC	
Gate-drain charge	Q_{gd}		9		nC	
Gate plateau voltage	$V_{plateau}$		6.6		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			1.1	V	$I_S=30\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		112		ns	$V_R=100\text{ V}$, $I_S=30\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		326		nC	
Peak reverse recovery current	I_{rrm}		4.8		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) $V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $L=0.3\text{ mH}$, starting $T_j=25\text{ }^\circ\text{C}$.

Electrical Characteristics Diagrams

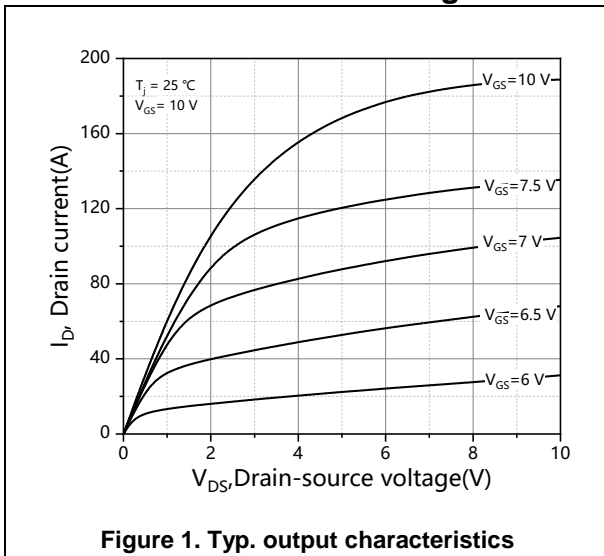


Figure 1. Typ. output characteristics

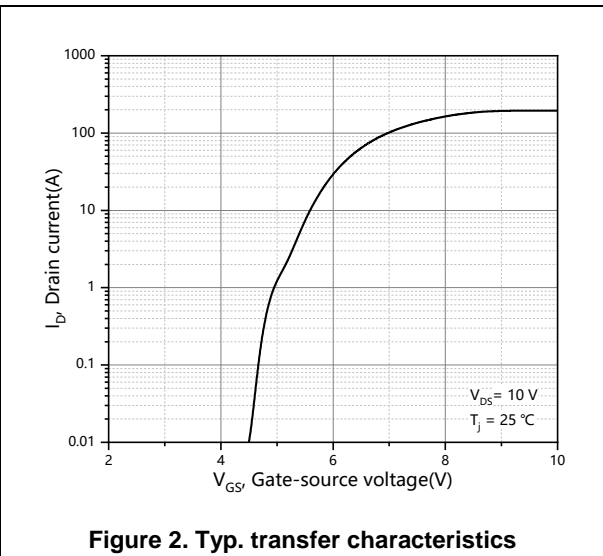


Figure 2. Typ. transfer characteristics

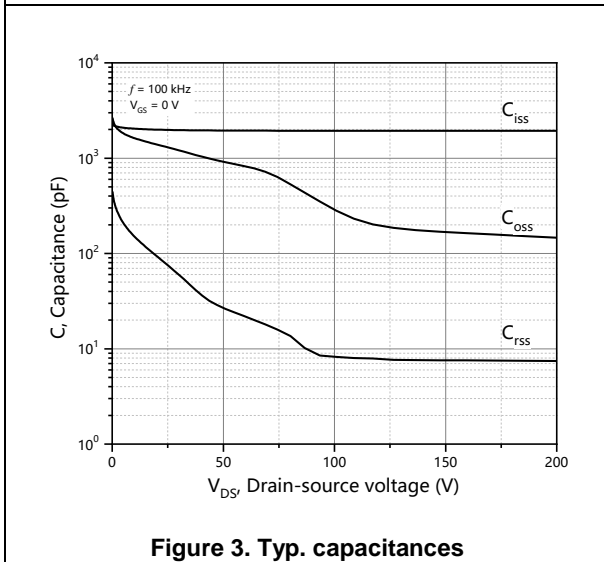


Figure 3. Typ. capacitances

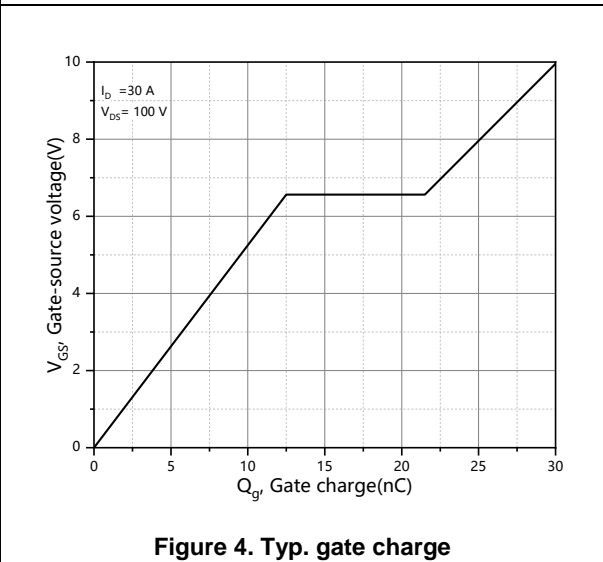


Figure 4. Typ. gate charge

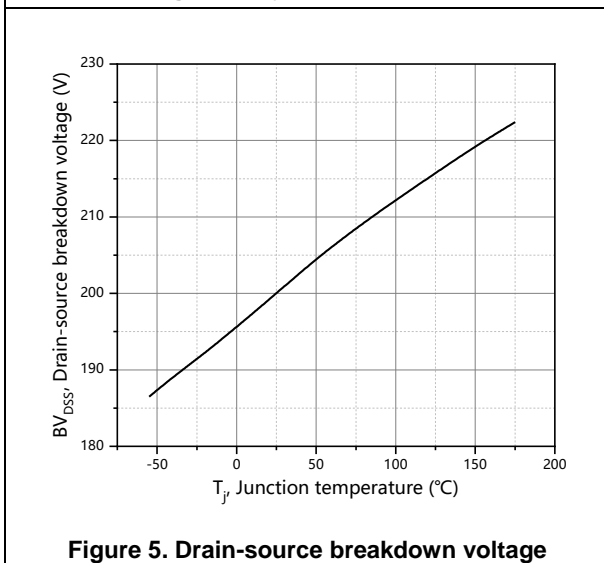


Figure 5. Drain-source breakdown voltage

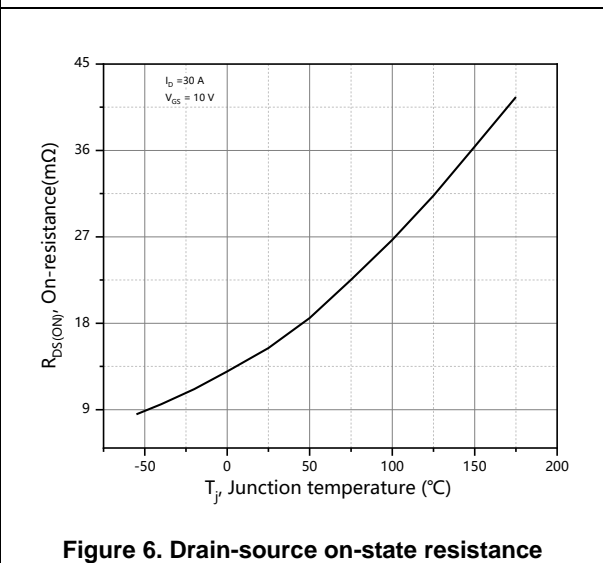
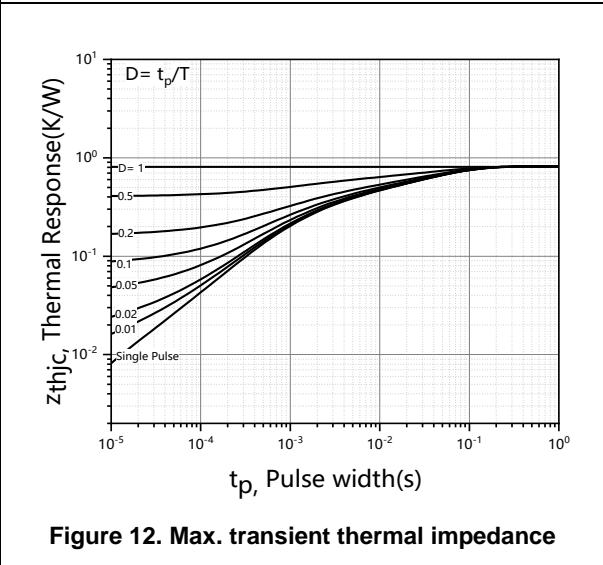
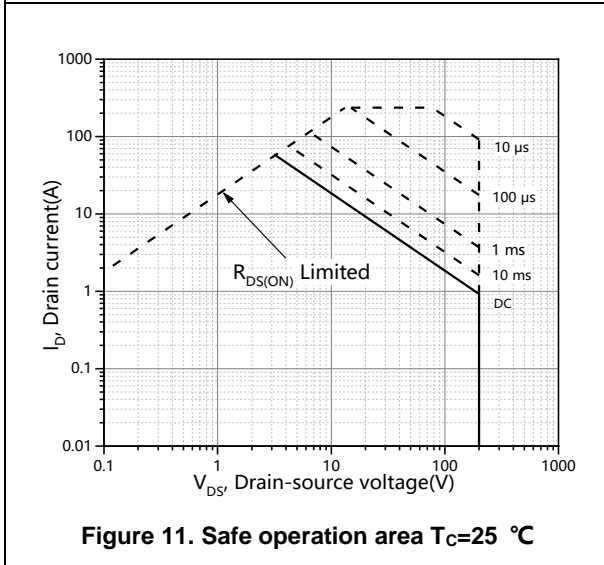
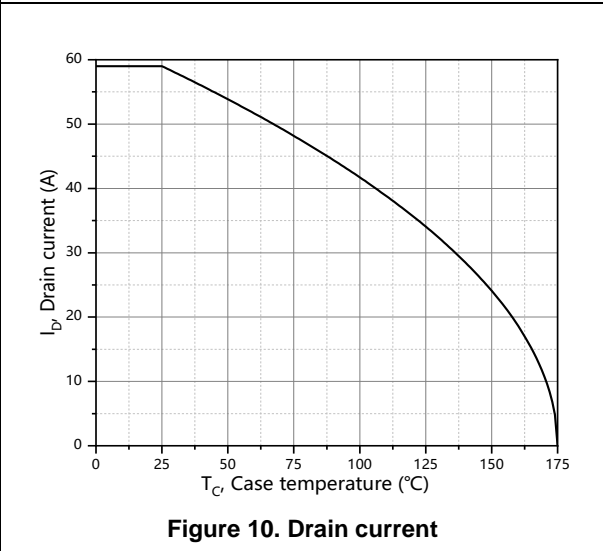
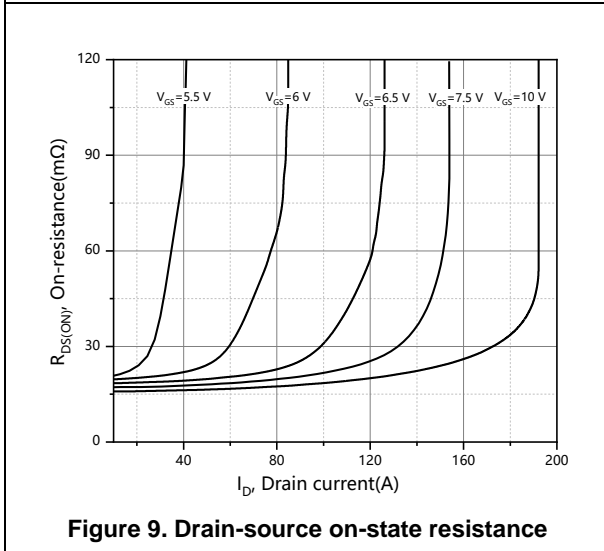
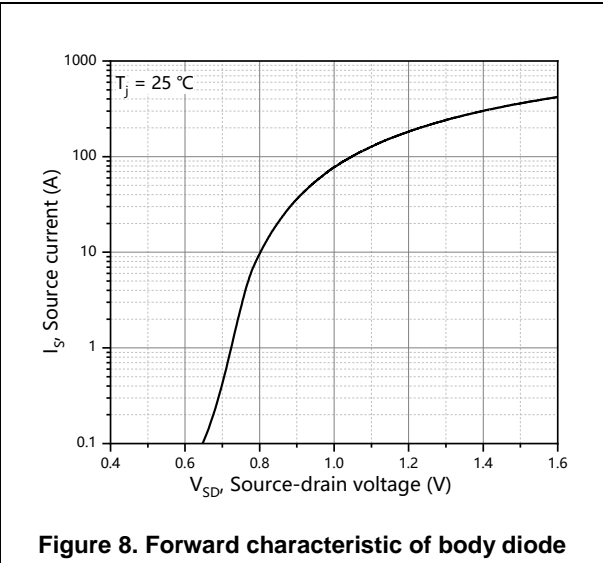
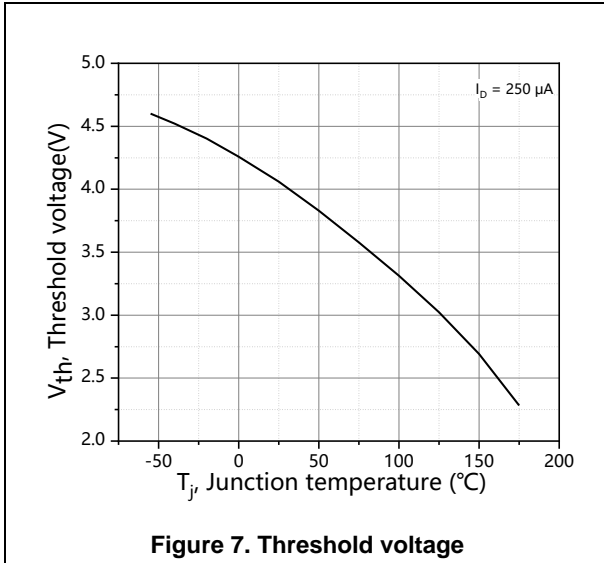


Figure 6. Drain-source on-state resistance



Test circuits and waveforms



Figure 1. Gate charge test circuit & waveform



Figure 2. Switching time test circuit & waveforms

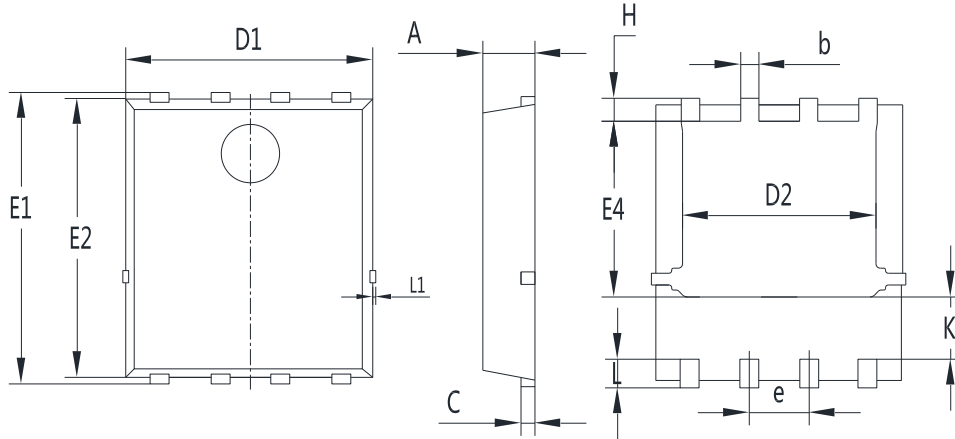


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms



Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm		
	Min	Nom	Max
A	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.154	0.254	0.354
D1	5.00	5.20	5.40
D2	3.80	4.10	4.25
e	1.17	1.27	1.37
E1	5.95	6.15	6.35
E2	5.66	5.86	6.06
E4	3.52	3.72	3.92
H	0.40	0.50	0.60
L	0.30	0.60	0.70
L1	0.12 REF		
K	1.15	1.30	1.45

Version :PDFN5*6-P package outline dimension

Ordering Information

Package Type	Units/ Reel	Reels/ Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
PDFN5*6-P	5000	2	10000	5	50000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
SFS20R20GNF	PDFN5*6	yes	yes	yes

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Revision History

Version	Revision History	Date
V1.0	Initial release	2025-03-10